

03DET22F1035

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| CLO1 (C3, PLO1) | COGNITIVE ASSESSMENT  (20 %) |  |
| CLO2 (P4, PLO5) | PSYCHOMOTOR ASSESMENT  (80 %) |  |
|  | TOTAL MARKS  (100%) |  |

**\*Refer to Rubric**

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| **1** | **LEARNING OUTCOMES (LO):**    1. Apply the simulation results for the various types of simulation analysis based on the electronic circuit theory and operations |
| **2** | **OBJECTIVE :**     1. Apply the simulation result for digital simulation analysis using the Truth Table. 2. Construct the digital schematics circuit and simulate the circuits using a particular simulation packages. |
| **3** | **THEORY :**    A digital circuit simulation is an event-driven, time-domain simulation. You can define an arbitrary time step for your live digital simulation and increment the simulation time discretely, one step at a time, and manually change the state of the input(s) at each time step.  Through the experiment, students can learn the concept of digital circuit simulation, applications of logic level simulation for combinational and sequential logic circuits. Logic inputs can be represented as Digital Clocks and output can be obtained by performing Time Domain Analysis. The analysis produced is displayed as a timing diagram and later can be represented into a Truth Table. |
| **4** | **EQUIPMENT / TOOLS / SOFTWARE :**   1. PC workstation 2. Related software |

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| **5** | **PROCEDURE :**  Draw and simulate this logic circuit below:  i. Circuit A: SYNCHRONOUS COUNTER ii. Circuit B: SHIFT REGISTER    **PART A: DIGITAL CIRCUIT**  Construct the Truth Table for each circuit based on timing diagram obtained in Result section.    **PART B: DIGITAL CIRCUIT SIMULATION**  Sketch the timing diagram for each circuit in result section.      Figure 5.1: Circuit A (SYNCHRONOUS COUNTER)       |  |  | | --- | --- | | Jc | A | | Kc | A | | Jb | 1 | | Kb | C | | Ja | C | | Ka | C | |
|  | Set the Digclock such as below :    DSTM1  Ontime = 0.5s  Offtime = 0.5s  Oppval = 1    DSTM2  Ontime = 20s  Offtime = 0.1us  Oppval = 1    DSTM3  Ontime = 20s  Offtime = 0.1us  Oppval = 1    Click **Menu Bar**, select **Analysis**\**Setup**. Click check box **Transient** to enable it and set the specifications as shown below:    Print Step : 0s  Final Time : 20s  No Print Delay : 0  Step Ceilling : 0    Click check box **Digital Setup** and click at **All 1**.  Simulate the circuit and observe the output waveform.    Sketch the timing diagram for each circuit in result section. |

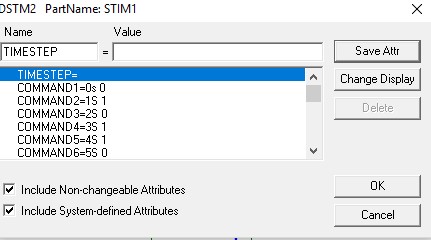
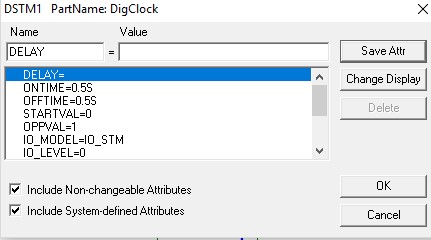
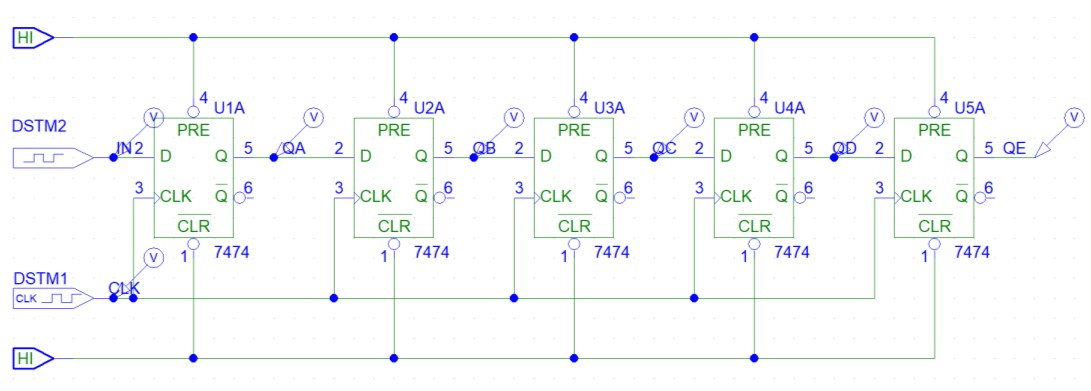
Figure 5.2:

Circuit B (SHIFT REGISTER)

DIG CLOCK SETTING

STIM1

SETTING



|  |  |
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|  | Click **Menu Bar**, select **Analysis**\**Setup**. Click check box **Transient** to enable it and set the specifications as shown below:    Print Step : 0.5s  Final Time : 20s  No Print Delay : 0  Step Ceilling : 0 |
| **6** | **RESULT :**   1. Timing diagram        1. Table 5.1: Truth Table for Circuit A (SYNCHRONOUS COUNTER)  |  |  |  |  | | --- | --- | --- | --- | | clock | Qa | Qb | Qc | | **0** | **0** | **0** | **0** | | **1** | **0** | **1** | **1** | | **2** | **1** | **0** | **1** | | **3** | **1** | **1** | **0** | | **4** | **0** | **1** | **0** | | **5** | **0** | **1** | **1** | | **6** | **1** | **0** | **1** | | **7** | **1** | **1** | **0** | | **8** | **0** | **1** | **0** | | **9** | **0** | **1** | **1** | | **10** | **0** | **0** | **1** | |

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|  | 1. Timing diagram        1. Table 5.2: Truth Table for Circuit B (SHIFT REGISTER)  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | | CLOCK | QA | QB | QC | QD | QE | | 0 | 1 | 1 | 1 | 1 | 1 | | 1 | 0 | 1 | 1 | 1 | 1 | | 2 | 1 | 0 | 1 | 1 | 1 | | 3 | 0 | 1 | 0 | 1 | 1 | | 4 | 1 | 0 | 1 | 0 | 1 | | 5 | 1 | 1 | 0 | 1 | 0 | | 6 | 0 | 1 | 1 | 0 | 1 | | 7 | 1 | 0 | 1 | 1 | 0 | | 8 | 1 | 1 | 0 | 1 | 1 | | 9 | 1 | 1 | 1 | 0 | 1 | | 10 | 0 | 1 | 1 | 1 | 0 | |
| **7** | **DISCUSSION :**  The digital circuit simulation experiment is a valuable tool for students to learn and apply the concepts of combinational and sequential logic circuits. By combining the simulation results with the truth table analysis, students can develop a comprehensive understanding of the circuit's behavior and validate its functionality.  The ability to represent logic inputs as digital clocks and perform time domain analysis is particularly useful for understanding the timing relationships and propagation delays within the circuit. This knowledge is essential for designing and troubleshooting more complex digital systems.  Furthermore, the use of simulation packages allows students to experiment with different circuit configurations, explore the impact of parameter changes, and gain practical experience in digital circuit design and analysis. This hands-on approach reinforces the theoretical concepts and prepares students for real-world applications in the field of digital electronics. |

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| **8** | **CONCLUSION :**  The digital circuit simulation experiment is a valuable tool for students to learn and apply the concepts of combinational and sequential logic circuits. By combining the simulation results with truth table analysis, students can develop a comprehensive understanding of the circuit's behavior and validate its functionality.  The ability to represent logic inputs as digital clocks and perform time domain analysis is particularly useful for understanding the timing relationships and propagation delays within the circuit. This knowledge is essential for designing and troubleshooting more complex digital systems.  Furthermore, the use of simulation packages allows students to experiment with different circuit configurations, explore the impact of parameter changes, and gain practical experience in digital circuit design and analysis. This hands-on approach reinforces theoretical concepts and prepares students for real-world applications in the field of digital electronics.  Overall, the digital circuit simulation experiment provides a valuable learning experience for students, enabling them to apply their knowledge, develop critical thinking skills, and gain practical expertise in the design and analysis of digital circuits. |

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| **PRACTICAL WORK 5: DIGITAL CIRCUIT SIMULATION** | | | | | | |  | A | B |
|  | **MATRIX NUMBER** | | | **NAME** | | |  |
|  |  | | |  | | |  |
| **A** |  | | |  | | |  |  |  |
| **B** |  | | |  | | |  |
| Course Learning  Outcomes(CLO)/  Learning Domain Cluster (CLS) | | Circuit | Skills /  Aspects | | Very Poor | Satisfactory | Very Good | Marks | |
| 1 | 2 | 3 |
| CLO 1 : Apply the simulation results for the various types of simulation analysis based on the electronic circuit theory and operations.    CLO 2: Construct the simulation and the PCB layout for digital and analogue circuits using a schematic capture software.    CLS 1:  Knowledge &  Understanding    CLS3a :  Practical skill | | PART  A    5.1 | **Draw circuit:** Student able to draw the circuit same as given. | | Able to draw the circuit with assistance. | Good to draw the  circuit moderately with little assistance. | Excellent to draw  the circuit effectively. | /3 | /3 |
| **Input and analysis setup:** Student able to set the input and transient. | | Able to set the input and transient with assistance. | Good to set the input and transient moderately with little assistance. | Excellent to set the input and transient effectively. | /3 | /3 |
| **Voltage and current display:** Student able to simulate the circuit and observe the result correctly. | | Able to simulate the circuit and observe the result correctly with assistance. | Good to simulate the circuit and observe the result correctly with little assistance. | Excellent to simulate the circuit and observe the result effectively. | /3 | /3 |
| **Timing Diagram:**  Student able to obtain the output for Qa, Qb and Qc correctly. | | Able to obtain the output Qa, Qb and Qc correctly with assistance. | Able to obtain the output for Qa, Qb  and Qc correctly  with little assistance. | Able to obtain the output for Qa, Qb and Qc effectively. | /3 | /3 |
|  | | | | |  | /12 | /12 |
| PART  B    5.2 | **Draw circuit:** Student able to draw the circuit same as given. | | Able to draw the circuit with assistance. | Good to draw the  circuit moderately with little assistance. | Excellent to draw  the circuit effectively. | /3 | /3 |
| **Input and analysis setup:** Student able to set the input and transient. | | Able to set the input and transient with assistance. | Good to set the input and transient moderately with little assistance. | Excellent to set the input and transient effectively. | /3 | /3 |
| **Voltage and current display:** Student able to simulate the circuit and observe the result correctly. | | Able to simulate the circuit and observe the result correctly with assistance. | Good to simulate the circuit and observe the result correctly with little assistance. | Excellent to simulate the circuit and observe the result effectively. | /3 | /3 |

# PRACTICAL SKILLS PSYCHOMOTOR ASSESMENT - (80%)

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| **NO.** | **STUDENT’S NAME** | **PART**  **A**    **(5.1)** | **PART**  **A**    **(5.2)** | **Total:** | **80%** |
| **(24 marks)** |
| **A** |  | /12 | /12 | /24 | /80 |
| **B** |  | /12 | /12 | /24 | /80 |

# PRACTICAL WORK COGNITIVE ASSESSMENT - (REPORT 20%)

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| --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | **Timing Diagram:**  Student able to obtain the output for QA, QB, QC, QD and QE correctly. | Able to obtain the output for QA, QB, QC, QD and QE correctly with assistance. | Able to obtain the output for QA, QB, QC, QD and QE correctly with little assistance. | Able to obtain the output for QA, QB, QC, QD and QE effectively. | /3 | /3 |
|  | |  |  |  | /12 | /12 |

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| **PART A TRUTH TABLE** | | **PART B TIMING DIAGRAM** | | **Discussion** | **Conclusion** | **TOTAL** | **20%** |
| 5.1 | 5.2 | 5.1 | 5.2 |  |  |  |  |
| /10 | /10 | /10 | /10 | /10 | /10 | /60 | /20 |

# TOTAL MARKS

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **NO.** | **STUDENT’S NAME** | **COGNITIVE**  **ASSESSMENT**  **(20 %)** | **PSYCHOMOTOR**  **ASSESMENT (80 %)** | **Total:** |
| **(100 %)** |
| **A** |  | /20 | /80 | /100 |
| **B** |  | /20 | /80 | /100 |